

Description

The XE6TSC5VU TVS diode is designed to protect high speed data interfaces. It has been specifically designed protect sensitive electronic components which are connected to data and transmission lines from overvoltage caused by ESD (Electrostatic Discharge), EFT (Electrical Fast Transients) and Lighting.

The XE6TSC5VU is in a SOT23-6L package and will protect four high-speed lines. It may be used to provide ESD protection up to $\pm 20\text{kV}$ Contact and $\pm 25\text{kV}$ air discharge according to IEC61000-4-2 , and withstand peak pulse current up to 40A(5/50ns) according to IEC61000-4-4 ,5A (8/20 us) according to IEC61000-4-5.

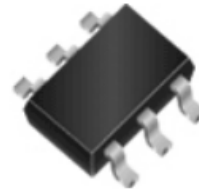
Features

- ◆ Working voltage: 5V
- ◆ Protect four I/O lines
- ◆ 100 Watts peak pulse power ($t_p=8/20\mu\text{s}$)
- ◆ Transient protection for data lines to IEC 61000-4-2 (ESD) $\pm 25\text{kV}$ (air), $\pm 20\text{kV}$ (contact)
- IEC 61000-4-4 (EFT)40A (8/20 μs)
- IEC 61000-4-5 (Surge)5A (8/20 μs)
- ◆ Low capacitance
- ◆ Low clamping voltage
- ◆ Low leakage current
- ◆ Solid-state silicon-avalanche technology

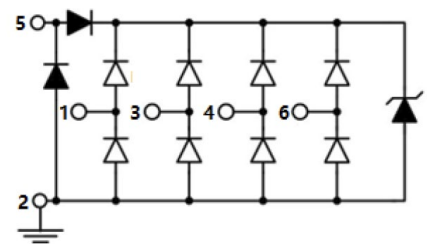
Applications

- ◆ USB 2.0 Power and Data Line Protection
- ◆ Video Graphics Cards
- ◆ Digital Visual Interface (DVI)
- ◆ 10/100/1000 Ethernet
- ◆ SIM Ports
- ◆ Notebook Computer
- ◆ Monitors and Flat Panel Displays
- ◆ IEEE 1394 Firewire Ports
- ◆ ATM Interfaces

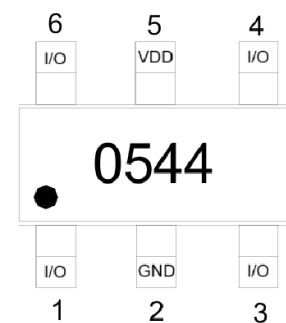
<http://www.xihangsemi.com>



SOT23-6L



Circuit Diagram



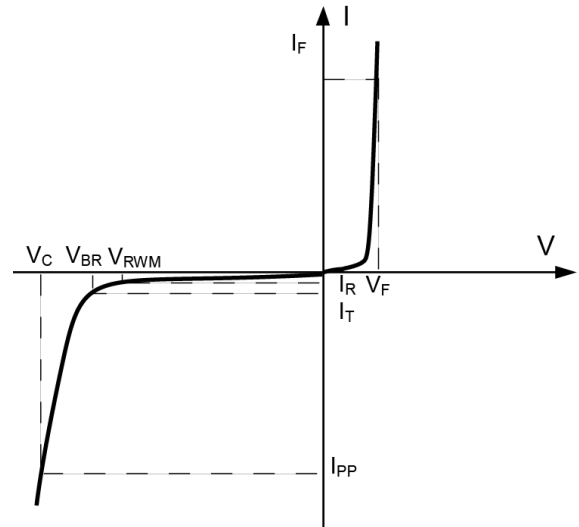
Marking

Order Information

Device	Package	Shipping
XE6TSC5VU	SOT23-6L	3000/Tape&Reel

Definitions of electrical characteristics

Symbol	Parameter
V_{RWM}	Reverse Stand-off Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Reverse Breakdown Voltage @ I_T
I_T	Test Current
I_{PP}	Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
I_F	Forward Current
V_F	Forward Voltage @ I_F
C_j	Junction Capacitance
I_{PP}	Peak Pulse Current



Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ($t_P = 8/20\mu S$)	P_{PK}	75	W
Peak Pulse Current ($t_P = 8/20\mu S$)	I_{pp}	5	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 25	kV
ESD according to IEC61000-4-2 contact discharge		± 20	kV
Lead Soldering Temperature	T_L	260 (10 sec)	$^{\circ}C$
Operating Temperature	T_{OP}	-55 to +125	$^{\circ}C$
Storage Temperature	T_{STG}	-55 to +150	$^{\circ}C$

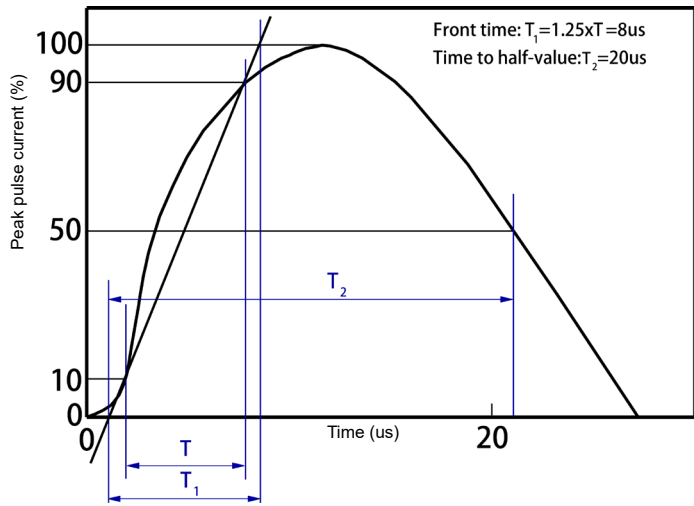
Electrical Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-off Voltage	V _{RWM}	Pin5 to Pin2			5.0	V
Reverse Breakdown Voltage	V _{BR}	I _T =1mA Pin5 to Pin2	6.0			V
Reverse Leakage Current	I _R	V _{RWM} =5V, T=25°C Pin5 to Pin2			1.0	μA
Forward voltage	V _F	I _T =15mA			1.2	V
Clamping Voltage ¹⁾	V _C	I _{PP} =1A t _P = 8/20μs Any I/O Pin to Ground		9.5	11	V
		I _{PP} =5A t _P = 8/20μs Any I/O Pin to Ground		12.5	15	V
		I _{PP} =13A t _P = 8/20μs V _{DD} to Ground		15	18	V
Junction Capacitance	C _{I/O - GND}	V _R =0V f = 1MHz, Any I/O pin to Ground		0.7	0.9	pF
	C _{I/O - I/O}	V _R =0V f = 1MHz, Between I/O pins		0.3	0.5	pF
	C _{VDD - GND}	V _R =0V f = 1MHz, Between VDD to GND		0.9	1.5	pF

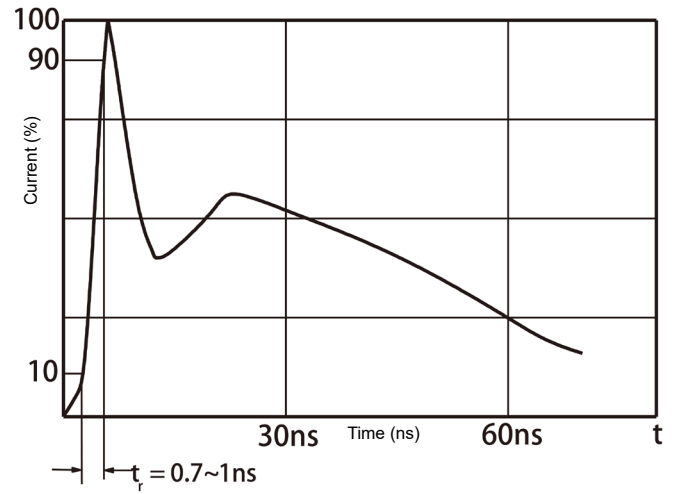
Notes:

1) Non-repetitive current pulse, according to IEC61000-4-5.

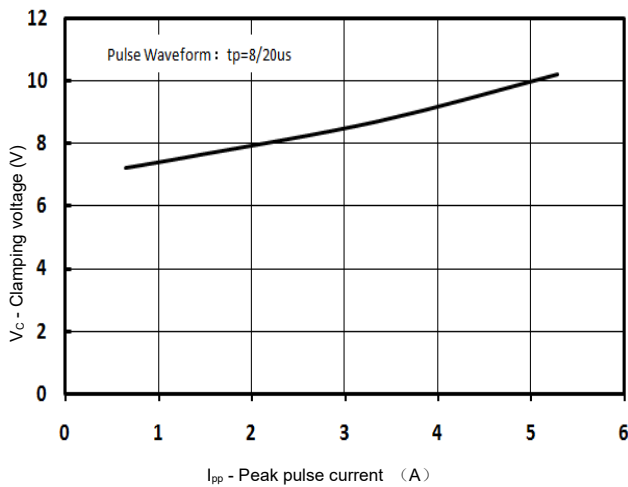
Typical Characteristics (Ta=25℃, unless otherwise noted)



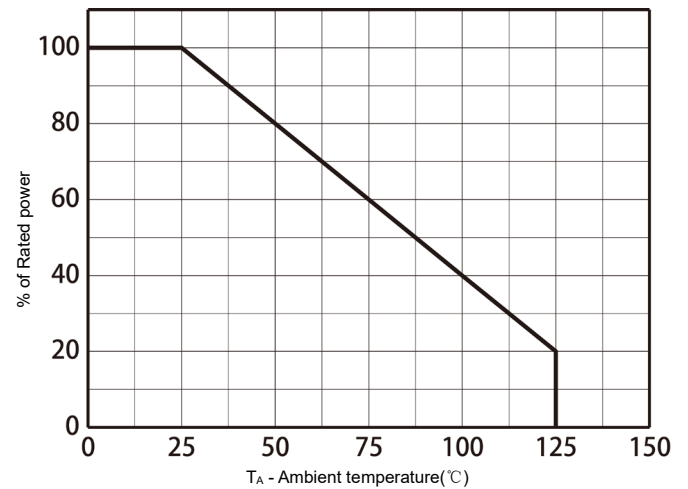
8/20 us waveform per IEC61000-4-5



Contact discharge current waveform per IEC61000-4-2



Clamping Voltage vs. Peak pulse current



Power derating vs. Ambient temperature

Application Information

The ESD protection scheme for system I/O connector is shown in Fig.1. In Fig.1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. The diode D3 is a back-drive protection design, which blocks the DC back-drive current when the potential of I/O pin is greater than that of VDD pin. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1 which may potentially damage any components that attached to VDD rail.

XE6TSC5VU has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage on the data line is small and protected IC will not be damaged.

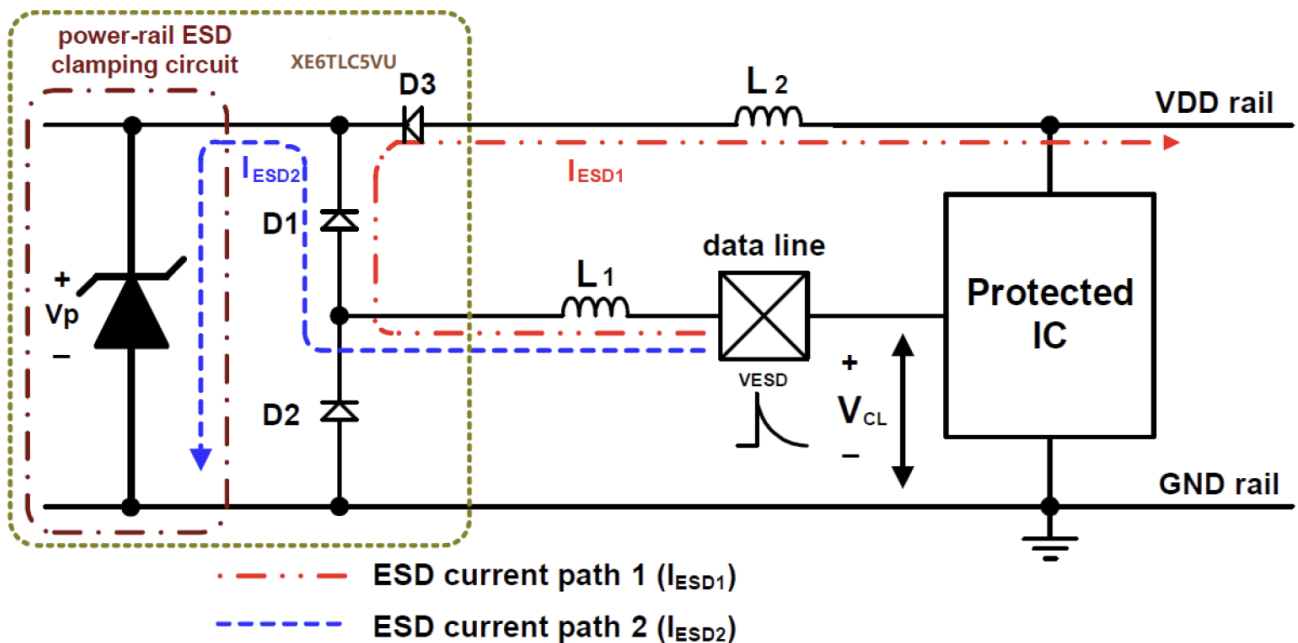
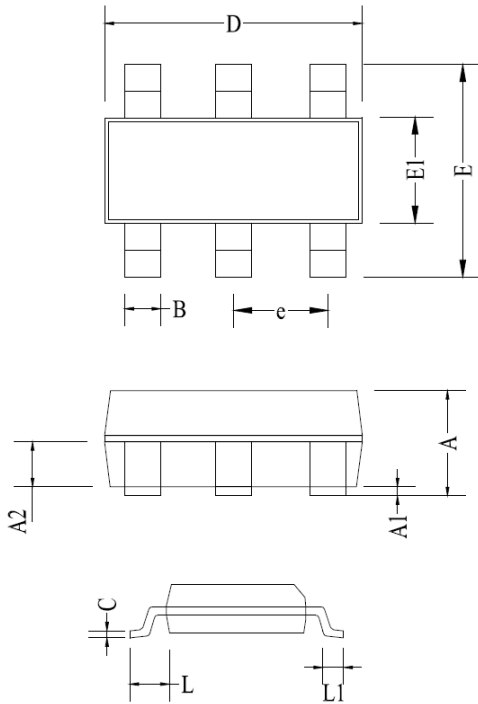


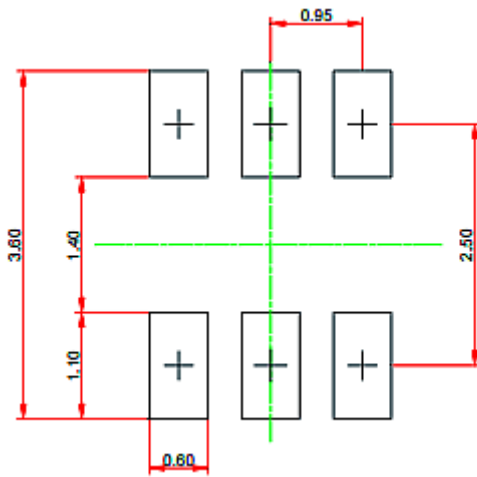
Fig. 1 Application of positive ESD pulse between data line and GND rail.

Package Outline Dimensions (SOT23-6L)



Symbol	Millimeter		Inches	
	Min	Max	Min	Max
A	0.90	1.45	0.035	0.057
A1	0.00	0.15	0.000	0.006
A2	0.45	0.65	0.017	0.026
B	0.35	0.50	0.010	0.020
C	0.08	0.20	0.003	0.007
D	2.80	3.00	0.110	0.122
e	0.69	1.02	0.032	0.043
E1	1.50	1.75	0.0060	0.0069
E	2.80BSC		0.110BSC	
L1	0.35	0.60	0.013	0.024
L	0.60		0.024	

Recommend Land Pattern (Unit: mm)



Note:

This recommended land pattern is for reference purpose only.

NOTICE

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